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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,270	12/30/2003	Saikumar Jayaraman	884.888US1	7480
59796 7590 05/05/2008 INTEL CORPORATION c/o INTELLEVATE, LLC P.O. BOX 52050 MINNEAPOLIS, MN 55402			EXAMINER TSOY, ELENA	
			ART UNIT 1792	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

***Advisory Action***

The Request for Reconsideration filed on April 18, 2008 under 37 CFR 1.116 in reply to the final rejection has been considered but is not deemed to place the application in condition for allowance for the reasons of record set forth in the Final Office Action mailed on 2/12/2008.

***Response to Arguments***

Applicant's arguments filed April 18, 2008 have been fully considered but they are not persuasive.

***§103 Rejection of the Claims***

Jacobson et al. in view of Suda et al. and Kamieniecki et al.

(A) Applicant believes that the citation to reference for a narrow purpose which fails to recognize what the reference teaches, is improper use of that reference. This action amounts to impermissible hindsight. Where the Office asserts it was known to fast test patterns on semiconductor wafers, the Applicant respectfully replies, the Applicant is not claiming a process having to do with semiconductor wafers. Where the Office Action inserts "etc." in the phrase "known to fast test patterns on semiconductor wafers, etc." The Applicant believes this "etc." is a catch-all to assert something that is not plainly taught or suggested in the combined references.

The Examiner respectfully disagrees with this argument. As to the Applicant not claiming a process having to do with semiconductor wafers, it is well settled that the reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem; and *there is no requirement that the prior art provide the same reason as the applicant to make the claimed invention*. Jacobson, Suda and Kamieniecki references relate to **semiconductor** wafers/devices.

As to improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the

time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

(B) The Final Office Action asserts that the Examiner never addressed the testing techniques because they were not recited in claims. The Applicant believes, however, the pending claims do recite testing techniques, e.g., "in situ testing the substrate [an imprinted polymer] while attached as part of an array of [imprinted polymer substrates]." (Claim 1). This language of "imprinted polymer" to define the substrate is in the plain text of claim 1.

The Examiner respectfully disagrees with this argument. The Examiner never addressed the testing techniques because the limitation "*in situ* testing the substrate" does not recite any *particular techniques* for testing.

(C) Applicant argues that the disconnect lies between Jacobson and the Suda and Kamieniecki references, where Jacobson's technology if applied to either of Suda or Kamieniecki, would destroy such inventions.

However, as was discussed in the previous Office action, the Suda and Kamieniecki references were applied not for their technologies but for the fact that the claimed concept of testing substrates *in situ* is not novel by itself. Testing *in situ* would not destroy Jacobson's technology.

Carter in view of Suda et al. and Kamieniecki et al.

Applicant argues that similarly to the above rejection involving Jacobson, the disconnect lies between Carter and the Suda and Kamieniecki references, where Carter's technology if applied to either of Suda or Kamieniecki, would destroy such inventions. Further, the "substrate" of Carter is not the "substrate" of either of Suda or Kamieniecki. Consequently, merely that of either of Suda or Kamieniecki may teach testing of their substrates, fails to show a teaching or suggestion to combine their technologies with Jacobson. Further, Carter would not look to either of Suda or Kamieniecki to solve any technical challenges or fields of endeavor.

The Examiner respectfully disagrees with this argument for the same reasons as discussed above in (C).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elena Tsoy whose telephone number is 571-272-1429. The examiner can normally be reached on Monday-Friday, 9:00AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Primary Examiner  
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May 2, 2008

/Elena Tsoy /

Primary Examiner, Art Unit 1792